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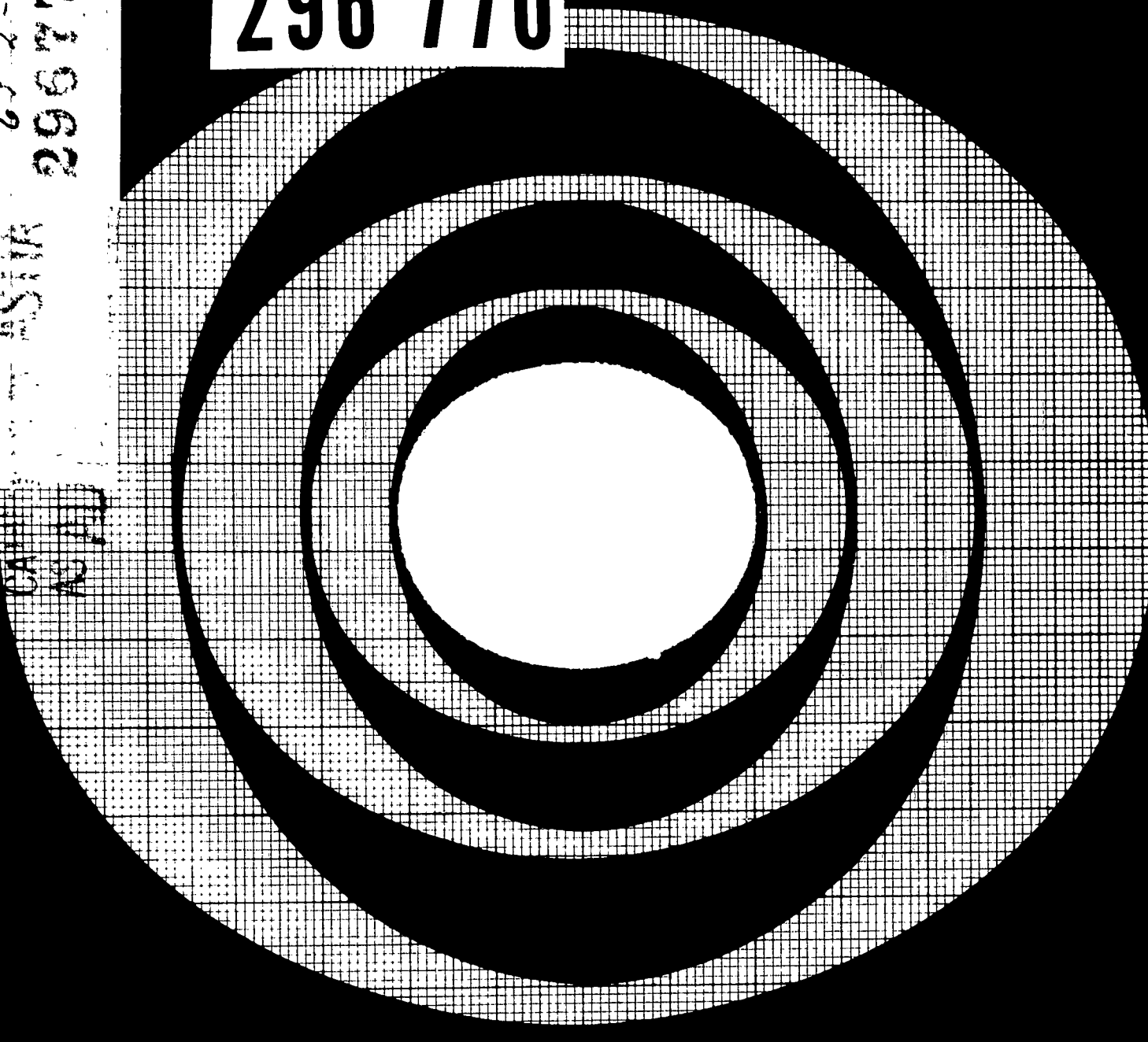

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SECOND QUARTERLY PROGRESS REPORT

Period:
31 July 1962 - 31 October 1962

PRODUCTION ENGINEERING MEASURE FOR THE IMPROVEMENT OF GERMANIUM ALLOY POWER TRANSISTORS

CONTRACT NO. DA-36-039-SC-86724

Placed by:
U.S. ARMY
ELECTRONICS MATERIEL AGENCY
Philadelphia
Pennsylvania

Contractor:

CLEVITE TRANSISTOR
A Division of Clevite Corporation
200 Smith Street
Waltham 54
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PRODUCTION ENGINEERING MEASURE FOR THE IMPROVEMENT OF GERMANIUM ALLOY POWER TRANSISTORS

SECOND QUARTERLY REPORT

31 July - 31 October 1962

Object:

Establish the capability to manufacture Germanium Alloy Transistors Types 2N297A, 2N1011 or 2N1120 with a maximum operating failure rate of 0.05% per 1,000 hours at a 90% confidence level as an objective.

SIGNAL CORPS CONTRACT NO. DA-36-039-SC-86724

Report prepared by George Wallis, Manager of Device Engineering Department of Clevite Transistor, A Division of Clevite Corporation.

Approved:

James F. Battey, General Manager

CLEVITE TRANSISTOR
A Division of Clevite Corporation
Waltham 54, Massachusetts

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SECOND QUARTERLY PROGRESS REPORT

PRODUCTION ENGINEERING MEASURE FOR THE IMPROVEMENT OF GERMANIUM ALLOY POWER TRANSISTORS

31 July 1962 - 31 October 1962

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I ABSTRACT

1 Extensive work was done on jet rinsing and experimental results are presented.

2 Work has been started on surface passivation by oxidation and experimental results are reported.

3 Experiments on surface passivation by organic coats have been started and results are given.

4 Further work on injection alloying indicated that control over the process is exceedingly difficult. It was therefore decided to stop further work on the process for the time being.

5 No work has been done on increase in emitter efficiency.

6 Steps have been taken which will make a 100% helium leak test feasible. In addition, the possibility is being explored of baking a thin coat of silicon resin onto welded units to close up microscopic leaks.

7 Some work has been done on the activation of calcium sulphate prior to encapsulation.

8 Measurements were made on punch-through limited transistors and results are discussed.

9 Correlation between storage and cut-off life tests are reported.

II PURPOSE

Production Engineering Measure (PEM) for improvement of production techniques to increase the reliability for the transistors designated below.

This shall include all work necessary to establish capability to manufacture the specified transistors utilizing the improved production techniques including all quantities of samples to be delivered, actual modification of production equipment to incorporate the improved technique, performance of the necessary tests to demonstrate the capability of the improved production line and the preparation and distribution of reports. The above work shall be performed for the following item:

Germanium Alloy Transistor types 2N297A, 2N1011 or 2N1120 with a maximum operating failure rate of 0.05% per 1,000 hours at a 90% confidence level at 95°C as an objective. The failure rate is an objective and as a minimum all process improvements specified below will be performed toward attaining or exceeding the specified failure rate.

PROCESSES TO BE IMPROVED

a. Cleaning Procedure

b. Surface Passivation by Oxidation

c. Surface Passivation by Organic Coats

d. Novel Method of Alloying

e. Increase in Emitter Efficiency

f. Hermeticity

III-1 CLEANING PROCEDURE AND SURFACE PASSIVATION BY OXIDATION

It is convenient to report on cleaning procedures and surface oxidation under the same heading, because our technique has been to perform matrix experiments with various cleaning and passivation treatments as variables.

As a start, efforts were made to work out a procedure which would produce distributions of I_{co}, I_{eo}, and gain at least equal to, or better than, those obtained by our present process.

The following variables were examined.

(1) Jet Rinse Conditions

Here we investigated hot and cold jet rinsing with high purity water, and the duration of jet rinsing. We also compared the following two procedures; i.e., 1) blowing off adhering water subsequent to the rinse, and 2) letting the water evaporate. According to early results, neither the temperature of the water rinsing nor the duration of the rinse in the range 20 seconds to 1½ minutes had any pronounced effects on the distributions of electrical parameters. There is some indication that it is beneficial to blow a unit dry (for instance, with a nitrogen blast) as soon as it has been rinsed.

(2) Baking Atmosphere

Primarily, we investigated oxygen and nitrogen under dry and wet conditions. Dry nitrogen and dry as well as wet oxygen appear to give similar results irrespective of whether the transistors received a final jet rinse. Wet nitrogen, on the other hand, seems to be inferior.

(3) Baking Temperature

So far, no significant differences have been detected for temperatures in the range 50°C to 125°C; however, this will be investigated more closely. Baking at 150°C clearly degrades the electrical characteristics and leads to inferior reliability

Transistors which have received these various treatments are now on life test so that possible differences in failure rate may be detected.

As an example of the type of distributions we obtained refer to Exhibit 1. I_{co} and I_{eo} at 60 volts and I_b at 2 amps and 2 volts are presented for transistors having received the following treatments.

A	Control	
B	Jet rinsed,	baked in N_2
C	Jet rinsed, dried in N_2,	baked in N_2
D	Jet rinsed,	baked in O_2
E	Jet rinsed, dried in N_2,	baked in O_2
F	Jet rinsed,	baked in wet O_2
G	Jet rinsed, dried in N_2,	baked in wet O_2

All units were jet rinsed with hot (180°F) high purity water and baked at 125°C overnight in the atmospheres noted above. The units were then welded and stabilized according to our standard procedure. The distributions for groups A to E look fairly similar. Groups F and G representing a bake in wet oxygen look somewhat poorer.

In comparing the pairs BC, DE and FG, the groups C, E and G which were dried with a blast of nitrogen are slightly superior to the groups B, D and F. The same trend was observed in similar runs.

In Exhibit 2 we show similar distributions for transistors having received the following treatments.

A Standard treatment (Control)

B Jet rinsed, nitrogen dried, baked in dry nitrogen

C Standard treatment , baked in dry nitrogen

D Jet rinsed, nitrogen dried, baked in dry oxygen

E Standard treatment , baked in dry oxygen

F Jet rinsed, nitrogen dried, baked in wet oxygen

G Standard treatment , baked in wet oxygen

In this case, the units were baked in the respective atmospheres at 100°C. Otherwise, processing was as for Exhibit 1.

The distributions for the seven groups differ somewhat in detail. Notice in particular the low collector leakage in transistors baked in dry oxygen. However, if we arbitrarily consider those transistors defective which have collector leakage currents above 1 ma then we find virtually no significant differences between the various groups. A comparison between the pairs BC, DE and FG suggests that the jet rinse has virtually no effect on initial distributions.

Unfortunately, during a period of approximately 6 weeks, a large percentage of transistors received for surface treatment had highly untypical electrical characteristics which tended to mask the effects of surface treatment and made proper interpretation of the experimental results quite hazardous. It therefore became necessary for us to investigate the reasons for the strange transistor characteristics.

Distributions of I_{co} and, to a lesser degree, I_{eo} and gain were abnormally spread out, BV_{ces} and BV_{ceo} traces were, in general, quite poor and emitter floating potentials were unreasonably high even at relatively low collector-to-base voltages. Since the floating potential is in most

cases quite insensitive to surface phenomena it became evident that the difficulties were associated with the bulk behavior of the transistors rather than with surface effects. This was further confirmed by the fact that repeated etching failed to improve the electrical characteristics. At this point we engaged in a program of failure analysis which indicated that a large percentage of these transistors had cracked dice. Further investigation showed that the cracking in most cases occurred subsequent to alloying, i.e. during soldering and, to a lesser extent, during welding. Steps have been taken to correct this situation and the incidence of cracking has been reduced by a large factor.

During this investigation we noted transistors which met the electrical specifications comfortably in every respect but nevertheless came under suspicion because of abnormally high floating potentials at voltages above the specified 60 volts. Some, but not all, of the transistors in this class were found to contain cracked dice. Evidently such transistors are poor reliability risks because it is to be expected that mechanical shock during repeated handling and thermal shock during life testing will produce further cracking resulting in sudden deterioration of electrical characteristics.

In the first quarterly report attention was drawn to the fact that in our transistors the incidence of a poor I_{co} characteristic was much higher than that of a poor I_{eo} characteristic. It was speculated that this may be due to the sheltered location of the collector junction which makes etching and clean-up more difficult than in the case of the emitter junction. It is now being realized that in many cases a relatively poor collector characteristic is due to a crack which passes through the collector edge but not through the emitter. Examples of such cracks are shown in Exhibit 3. There are several ways in which these cracks may arise. For

instance, some of the cracks may be produced during the scribing of the dice and may spread during subsequent processing. Another possibility is that the base ring, not being a perfect thermal match to the germanium, can generate cracks as a consequence of thermal shock during soldering. A further possibility is mechanical shock which produces cracks in the regions where the etched die is thinnest and without mechanical support, i.e. between emitter and base ring. This matter is under continuing investigation since cracking affects not only yield but also reliability.

III-2 SURFACE PASSIVATION BY ORGANIC COATS

Silane coating, like most chemical processes, involves a considerable number of variables.

Before making a detailed investigation of a particular version of the silane coating process, it seemed desirable to make a preliminary evaluation of a limited number of likely process combinations.

For a starting point, the silane process selected was that used on our alloyed and mesa silicon diodes.

The initial procedure was as follows:

(1) The transistors were placed in bottles with gaskets and holes in the covers, so that only the region within the weld ring was exposed.

(2) After inserting the transistors the chamber was flushed @ 5 cfh with humid (50% RH) nitrogen for 45 minutes.

(3) Two cc of a mixture of: 2 parts chloro-trimethyl silane
9 parts dichloro-dimethyl silane
9 parts trichloro methyl silane
were added to the silane flask, and the nitrogen stream diverted from the humidification train to the silane bottle and then to the chamber.

(4) After three minutes the units were removed and placed in a 95°C oven for two hours.

(5) The units were covered with acetone, boiled three minutes and decanted.

(6) The acetone boil was repeated for a total of three times.

(7) The units were then baked for two hours at 95°C.

For purposes of evaluation, the following criteria were selected:

(1) No serious degradation of electrical characteristics should occur as compared with reference uncoated units.

(2) The coating should be as impermeable as possible to keep extraneous material out of effective range of the junction edge. Here the effect of 100 percent humidity, for a few seconds, on the electrical characteristics was used as a qualitative measure.

All initial testing reported here was done on open units, including a 145° bake. The risks involved were taken to permit access for checking coating permeability. Current coated units, however, are being capped and will be tested after standard baking and accelerated life tests.

Results are indicated subsequently along with the appropriate coating variables. As sometimes happens, testing for more parameters in the early stages of the work would have been helpful. In particular, some lots with an abnormally high number of faulty units made it difficult to draw significant conclusions.

It should be pointed out here that to date coated units have not been significantly better electrically than the reference units, except when exposed to high humidity.

Of the many coating procedures possible, the following were varied in at least one of the sample groups:

(1) Recoating

Coatings with multiple thin layers tend to have superior adherence and impermeability as compared to a single layer coating. This was tested in four cases where one or more additional coats were added to part of the units. In two of the four cases improvement was probable, the other cases being inconclusive.

(2) Dry Flush

The general premise was that it would be better to have the silane reaction occur on the surface of the unit rather than in the atmosphere. This would avoid the deposition of coagulated "Blobs." Accordingly, a short two to five minute "Dry Flush" was interposed between the humidification period and the introduction of silane. Here improvement seemed quite certain in the first two cases and the "Dry Flush" was included in most of the subsequent runs. Omission of the "Dry Flush" in two subsequent cases was inconclusive. It should be pointed out that the mechanism might well have been reduction of surface moisture content to a level nearer to optimum. Results on the length of the humid flush and ethyl silicate undercoating tend to support the latter hypothesis. It is planned to revise the set-up so that wet and dry nitrogen can be blended to bring lower humidities under better control.

(3) Humid Flush Times

This factor varied from five minutes to over a weekend. Results probably favor the short flush time.

(4) Humid Flush after Silane

The intent in adding this step was to insure that hydrolysis, removing all the chlorine radicals, was complete. In two lots split in this respect no difference was observed. In retrospect this might have been expected since plenty of moisture was available in the subsequent "laboratory air" bake of the coating.

(5) Acetone Boil

During the silane reaction hydrochloric acid is formed which can form chlorides with the solder components. Their removal in this step is expected due to their slight solvability in the warm acetone. The possibility of doing more harm than good by spreading them around was considered and so the step was omitted on several lots. Results here are particularly confusing with large electrical changes occurring on some lots and little or none on others.

(6) Ethyl Silicate

Ethyl silicate is a potential alternative to silane as a coating material. Its hydration gives only volatile ethyl alcohol and silica that is more or less hydrated. Results of one lot have electrical characteristics equivalent to the controls. Imperviousness to moisture seems to be less than that of the better silane coating.

(7) Silane over Ethyl Silicate

This combination is of interest because of the expected ability of the silane to complete the dehydration of the underlying silica coat. Two lots processed in this manner look good.

(8) Ethyl Silicate over Silane

One lot with this combination is clearly poor.

(9) Extended 95° Bake after Acetone Boil

It was noticed on one lot that the loss in gain, due to the acetone boil, was partially recovered by a few days at 95°C. Comparison of a 15 minute versus an overnight 95° bake before a 145° treatment indicate a probable preference for the longer bake.

Emphasis on the coating work is now shifting to larger lots of the more promising coatings and better preselection of the units. This will come at the expense of testing at intermediate steps of the process but will provide increasing significance to the net overall effect of the better coatings.

The trends of electrical parameters through coating and capping are shown in the distributions of Exhibits 4 and 5. They represent good silane and ethyl silicate coatings. Included are data from a control group, from the same transistor lot, but not coated. No significant differences are shown between the behavior of the coated versus uncoated units.

III-3 INJECTION ALLOYING OF GERMANIUM POWER TRANSISTORS - B. Ritter

A. Thermal Control

It was found that the small inertia of the carbon boats and reservoirs made it difficult for the controller to maintain and follow the set point at the maximum alloying temperature and during the cooling cycle. The temperature of the boats would change so quickly that the controller was constantly overcorrecting, producing an oscillatory heat-cool cycle with the desired temperature as the average. In order to eliminate this $\pm$ 4° to 5°C oscillation, a forced thermal cycle was adopted.

Here, the high frequency generator was controlled by a powerstat that was set for the desired maximum temperature. When this temperature was reached, a motor started driving the powerstat set point down. By starting with the same maximum temperature setting each time and leaving the motor at the same speed, almost identical cycles could be had for each run.

B. Cooling

Better thermal control allowed experiments on cooling to be carried out. It was found that in order to obtain smooth, homogeneous alloyed regions, it is necessary to cool the boats at a rate of 25°C/minute or slower. The heating rate apparently is not critical providing there is no temperature gradient through the boat at the injection point.

C. Boat Orientation

During the first quarter most alloying was done with the boat mounted vertically. At the beginning of the second quarter the boats were mounted horizontally to see if this would improve alloying. A number of units were made with injection at alloying temperature rather than at the usual low temperatures. The alloy short through

the center of the die that usually occurred with high temperature injection into vertically mounted boats was absent from these units, indicating that the shorting is not only due to high temperature indium impinging on the die center as was previously thought. Rather, in most cases, it was produced during cooling because the indium did not break in the sprue connecting the die cavity and reservoir. When the boats were in the vertical position, the weight of the indium in the upper reservoir prevented the breaking of the connecting indium, thus a hole would be dissolved through the center of the die.

Higher temperature injection with the boats mounted horizontally seemed to improve wetting and produced smoother junctions with fewer irregularities. In particular, it became possible to produce flat, smooth collectors with good alloyed regions, about 1 mil thick. The emitters, however, were wavy and usually were alloyed deeper around the periphery than in the center. Also, the emitter alloyed regions were poorly regrown. This type of difficulty is encountered whenever one alloys to a depth of more than 1 to 1½ mils and is due to temperature gradients across the boats.

It should be emphasized that none of the injection-alloyed junctions were as uniform as a good junction produced by conventional methods. Furthermore, reproducibility was relatively poor on account of numerous mechanical problems that proved hard to control.

Since it appears now that this approach is unlikely to produce favorable results during the life of this contract, work along these lines has been suspended. Instead, areas will be investigated which appear to be more fruitful and have a more immediate bearing on the reliability of transistors.

III-4 HERMETICITY - Edward J. Fradsham

As discussed in the first quarterly report, helium leak detection is far more sensitive than our present methanol leak test. We are therefore, attempting to work out a procedure which will make a 100% helium leak test feasible. In our first approach, welded transistors were pressurized in helium so that the latter could diffuse into the can when leaks were present. The transistors were then flushed in nitrogen and tested in a helium leak detector. However, one cannot be certain that during the nitrogen flush all helium will be removed from crevices. If any helium remains trapped, it will produce misleading readings in the detector. Hence, the following alternative procedure is being tried out. In the past, the desiccant which is to be placed into a package prior to capping has been stored under an atmosphere of dry nitrogen. As a trial, the desiccant will instead be stored in a helium atmosphere. The expectation is that enough helium will be absorbed by the desiccant so that a capped unit will contain a significant amount of helium and can be leak tested.

Another approach to the hermeticity problem is being investigated. A thin film of silicone resin is deposited on capped units by dipping and then baked on at approximately 100°C. It is hoped that in addition to sealing off small leaks the film will also provide improved resistance to salt spray corrosion.

Very preliminary data indicate that the percentage of leakers is probably significantly different among units that pass and units that fail during storage life tests. After a 5000 hour storage test at 125° (100° for a few units) 15 failures and 14 good units, selected at random, were pressurized in helium and tested for leaks. If we define as leakers units having a leak rate greater than 10^{-7} std cc/sec, then as shown in Exhibit 6, there were 7 leakers among the rejects and 4 leakers among the units that had passed the life test. This experiment will be followed up with larger lot sizes.

III-5 INCREASE IN EMITTER EFFICIENCY

There has been no activity in this area.

III-6 ACTIVATION OF DESICCANT - B. Ritter

In our present procedure, calcium sulphate is being used as a desiccant. Prior to encapsulation, the desiccant is baked at temperatures between 150°C and 180°C for 12 hours in nitrogen. An investigation was started to find out whether activation of the calcium sulphate at higher temperatures would produce improved results. Experimental baking was done at temperatures in the range 170°C to 260°C. Changes in the appearance of the powder were noted above 200°C. As for electrical characteristics, results were heavily masked by the previously discussed high incidence of cracked dice. Nevertheless, there is a suggestion that activation around 200°C gives optimum electrical results.

In some experiments, desiccant was omitted from the package. This resulted in a high degree of instability. In particular, the I_{co} trace as observed on a curve tracer improved as the transistors were swept out to progressively higher voltages. The effect was reminiscent of a familiar phenonenom with many semiconductor devices which is sometimes referred to as "pushing." It is attributed either to ion movement or polarization of more or less stationary molecules under the action of an electric field near the junction. Attempts to suppress "pushing" by modifications in surface treatment have not been successful, so far.

III-7 LIFE TESTS - B. Burman

It was felt that no useful purpose would be served by setting up elaborate life tests for transistors which were made during the period when cracking of dice represented a severe problem. As soon as more typical transistors began to become available, a day's production was set aside for the following correlation experiment which is now in progress.

Storage tests at 95°C, 125°C, 135°C, 145°C, 180°C.

Cut-off life tests at 85°C, at various collector-to-base voltages up to 80% of the breakdown voltage.

Accelerated life test with temperature in 20°C intervals as the stress.

One phase of the contract involves correlating storage with cut-off life, the storage life test being a temperature stress test, while the cut-off life is a combination of a temperature and voltage stress.

The first experiment consisted of 180 units @ 100°C on storage life, and 60 each on cut-off life at stress levels of V_{CE} = 20V, 30V, and 40V; V_{BE} = + 0.2V @ 55°C.

The data were fed into an IBM 1620 computer evaluating the mean, standard deviation, variance, minimum and maximum readings, and the range of the values. Exhibits 7 - 9 plot the "Mean" and "Standard Deviation" comparing storage with cut-off life.

First indications, as seem by the graphs, are that the cut-off life tests closely approximate the storage life @ 100°C.

Cut-off life tests at higher voltage stresses are presently being initiated and will be evaluated for utilization as accelerated life tests.

III-8 PUNCH-THROUGH LIMITED TRANSISTORS - George Wallis

On the suggestion of B. Reich of the Signal Corps, a large number of transistors having relatively low punch-through voltages were examined under conditions of BV_{ces} and BV_{cex}. For the most part, observations were made on a 60 cycle curve tracer, with a more suitable circuit being under construction. As expected, breakdown set in near the punch-through voltage irrespective of the emitter-to-base voltage. It was also confirmed that the current-voltage characteristic in the breakdown region was less dependent on the emitter-to-base voltage in punch-through limited devices than is the case with conventional transistors. However, attempts to observe secondary breakdown as a function of emitter-to-base voltage were largely unsuccessful. Where a true secondary breakdown was observed at all, it proved to be destructive so that repeated observations on a transistor were not feasible. In most cases, we observed a hysteresis loop rather than a true secondary breakdown trace. The hysteresis loop or "balloon" is clearly a thermal effect in that at a given low emitter-to-collector voltage the collector current is much larger after ballooning had occurred than prior to ballooning. Thus, a "balloon" like a secondary breakdown probably originates from a hotspot. However, in the case of the secondary breakdown, the spot appears to get hotter than in the case of a "balloon" as evidenced by 1) its destructive nature, and 2) the drop in voltage to a relatively low value. By contrast, a "balloon" is usually not destructive and the drop in voltage is less severe. Furthermore, after "ballooning" appreciable cooling of the spot occurs within a cycle whereas after secondary breakdown the spot apparently remains hot for the rest of a cycle.

With punch-through limited transistors, "ballooning" occurred more nearly at the same current level irrespective of emitter-to-base voltage than with transistors which were not punch-through limited. However, with emitter-to-base voltage equal to zero (BV_{ces}), "ballooning" appeared to set in at lower currents with punch-through limited transistors than with transistors from the same lot which were not punch-through limited.

IV CONCLUSIONS

The following conclusions are drawn from the work during the second quarter.

1. At the end of the first quarter, we stated that a comparison between conventionally rinsed and jet rinsed transistors indicated no significant difference between the two groups as far as I_{co} and I_{eo} were concerned; the control groups had somewhat lower values and a tighter distribution of I_b than the jet rinsed groups. During the second quarter rinsing equipment with higher flow rates was used and as a result differences in I_b between controls and experimental groups have disappeared, i.e., we now see no significant differences in any respect. Life test results on groups handled during the second quarter will shortly become available.

2. Bakes prior to encapsulation at various temperatures and in various atmospheres have given rather inconclusive results. There is a suggestion that a bake in dry oxygen at around 100°C gives superior results.

3. Transistors have been coated with silane under various process combinations. The best coated groups have had electrical characteristics equal to the control groups. These have been put on life test and results will become available shortly.

4. Injection alloying presents many difficult control problems. At present there is no evidence that injection-alloyed junctions are superior to junctions made by conventional techniques.

5 Steps are being taken so that helium leak-testing can be performed on a 100% basis.

6 Initial experiments on the optimum activation procedure for the desiccant indicated that a bake at about 200°C gives best results.

7 A comparison was made of storage life at 100°C and cut-off life at 55°C with V_{CE} = -20V for 2N456A types, V_{CE} = -30V for 2N457A types, and V_{CE} = -40V for 2N458A types. No significant differences were observed between storage life and cut-off life under these conditions.

8 Comparison of BV_{cex} in punch-through limited and conventional transistors has indicated the following. (i) On a 60 cycle sweep, the secondary breakdown occurs but rarely and then is usually destructive. (ii) In place of secondary breakdown we commonly observe thermally induced hysteresis or "ballooning" which appears to be essentially the same physical phenomenon as secondary breakdown but is almost invariably non-destructive. With punch-through limited transistors, "ballooning" tends to set in at lower currents but is less affected by emitter-to-base voltage than is the case for conventional transistors.

V PROGRAM FOR NEXT QUARTER

1. Latest results on jet rinsing have suggested that the rinse is either ineffective or that its effects are being masked. If these results can be confirmed, no further work on jet rinsing will be done at least for the time being.
2. There is a suggestion that a dry oxygen bake is beneficial. An effort will be made to either confirm or disprove the conclusion.
3. Work on silane coating will continue.
4. An evaluation will be made of a helium leak test on a 100% basis along the lines described in the text.
5. Work on punch-through limited transistors will continue.
6. Work on the activation of calcium sulphate will receive high priority.
7. An attempt will be made to correlate storage tests at various temperatures, cut-off tests at various voltages and accelerated tests with temperature as the stress, as described in the text.

VI PUBLICATIONS AND REPORTS

No publications and reports have resulted from or about this contract.

VII IDENTIFICATION OF TECHNICIANS

John Kelly has been substituted for Jean Madden and Noble Hamilton has been added to the other engineers working on this Contract.

The following engineers worked on the Contract during the second quarter:

Bruce Burman - Quality Control Engineer. Mr. Burman received his B.S. in electrical engineering in 1960, from Lowell Technological Institute, Lowell, Massachusetts, and in that year joined Clevite Transistor as a trainee. He completed training assignments in Instrumentation, Sales and Quality Control, and in 1961, was permanently assigned as a Quality Control engineer. Since that time, Mr. Burman has carried out production evaluation on power transistors with emphasis on environmental and life test performance.

Edward Fradsham - Manager of Process Control Inspection. Mr. Fradsham is a registered professional engineer in the Commonwealth of Massachusetts. From 1942 to 1957, he worked in the capacity of inspection planner in the General Electric Company, Everett, Massachusetts. In 1957, he joined the Clevite Transistor, Quality Control Department and has worked in a number of capacities both in Incoming and In-process Inspection.

Noble E. Hamilton - Project Engineer. Mr. Hamilton received his B.S. in chemical engineering in 1943 from Iowa State College. From 1953 to 1955, he worked in the capacity of metallurgical supervisor at Consolidated Vacuum Corp., Rochester, New York. In 1955, he joined Clevite Transistor, Materials and Metallurgy Department, as a senior metallurgist. In 1961, he was promoted to project engineer.

John I. Kelly - Device Engineer. Mr. Kelly received his B.S. in physics in 1959 from Queens University, Belfast, N. Ireland. From 1959 to 1961, he worked in the capacity of physicist for Mullard, Ltd., Millbrook, Southampton, England. From 1961 to 1962, he worked in the capacity of physics teacher for Middlesex Education Authority, London, England. In September, 1962, he joined Clevite Transistor and was permanently assigned to the Device Engineering Department.

Barry Ritter - Device Engineer. Mr. Ritter received his B.S. degree in mechanical engineering in 1962, from Rensselaer Polytechnic Institute, Troy, New York. He joined Clevite Transistor as a trainee in March, 1962, and was permanently assigned to Device Engineering in September, 1962.

George Wallis - Manager of Device Engineering. He received his PhD in Physics in 1953, from Brown University, Providence, Rhode Island. From 1953 to 1958, he worked at Sylvania Electric Products in Woburn, Massachusetts. In 1958, he joined Clevite Transistor as Manager of Advanced Development, and in 1960 he became Manager of the Device Engineering Department.

Engineering Hours - During the quarter, 1,263 hours were expended by salaried personnel; 896 hours were expended by hourly personnel.

VIII LIST OF FIGURES

Exhibit 1 Distributions of I_{co}, I_{eo} and I_b for various surface treatments.

2 Distributions of I_{co}, I_{eo} and I_b for various surface treatments.

3 Microphotographs of cracks which affect collector but not emitter.

4 Distributions of I_{co}, I_{eo} and I_b of silane coated and control groups.

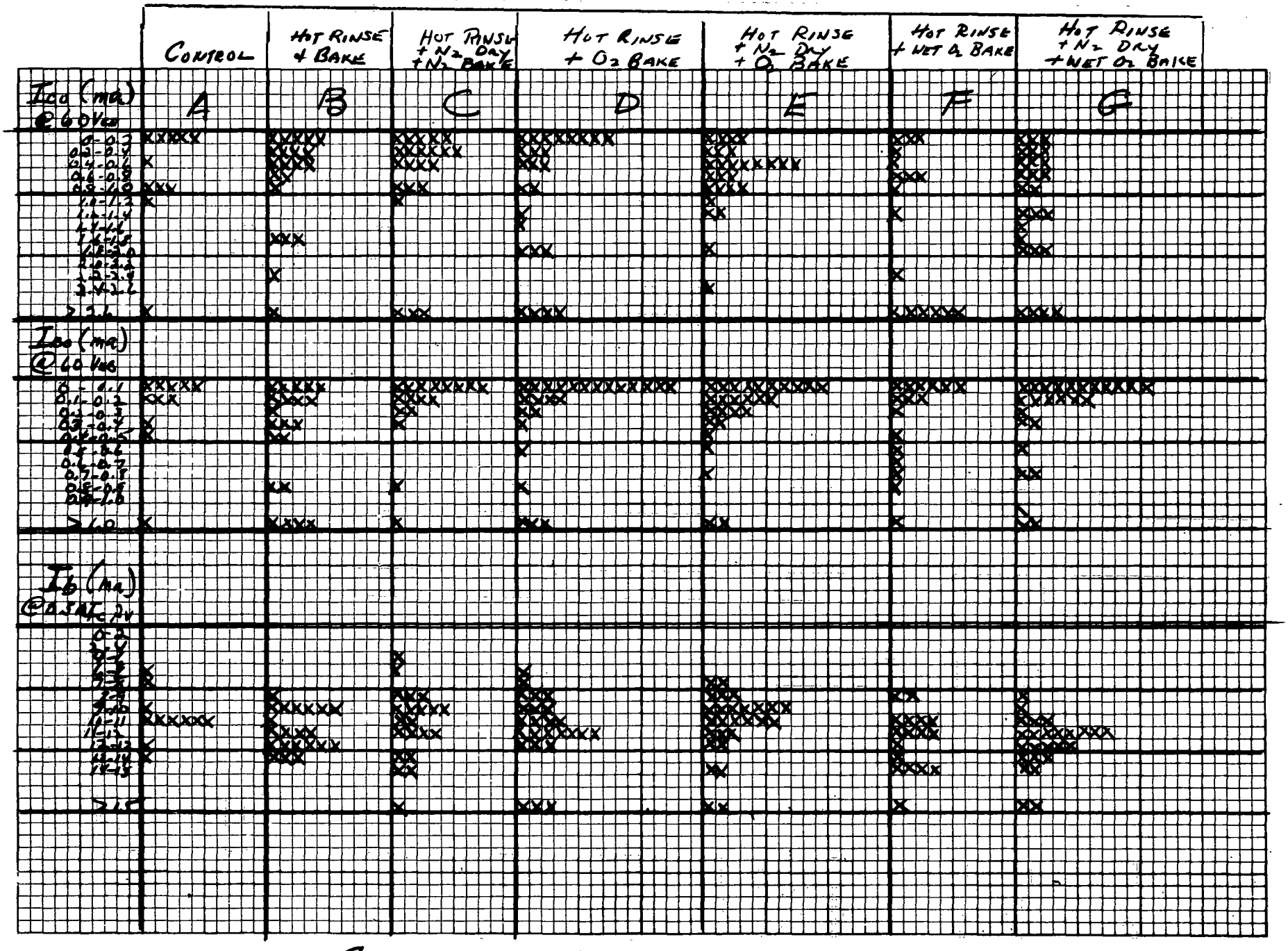
5 Distributions of I_{co}, I_{eo} and I_b of ethyl silicate and control groups.

6 Life test data as a function of leak rate.

7 Mean and Standard Deviation of I_{CBO} and H_{FE} versus 1000 hours operating and cut-off life, 2N456A

8 Mean and Standard Deviation of I_{CBO} and H_{FE} versus 1000 hours operating and cut-off life, 2N457A

9 Mean and Standard Deviation of I_{CBO} and H_{FE} versus 1000 hours operating and cut-off life, 2N458A



GROUP 13- A-CONTROL

EXHIBIT 1

EXP. 15

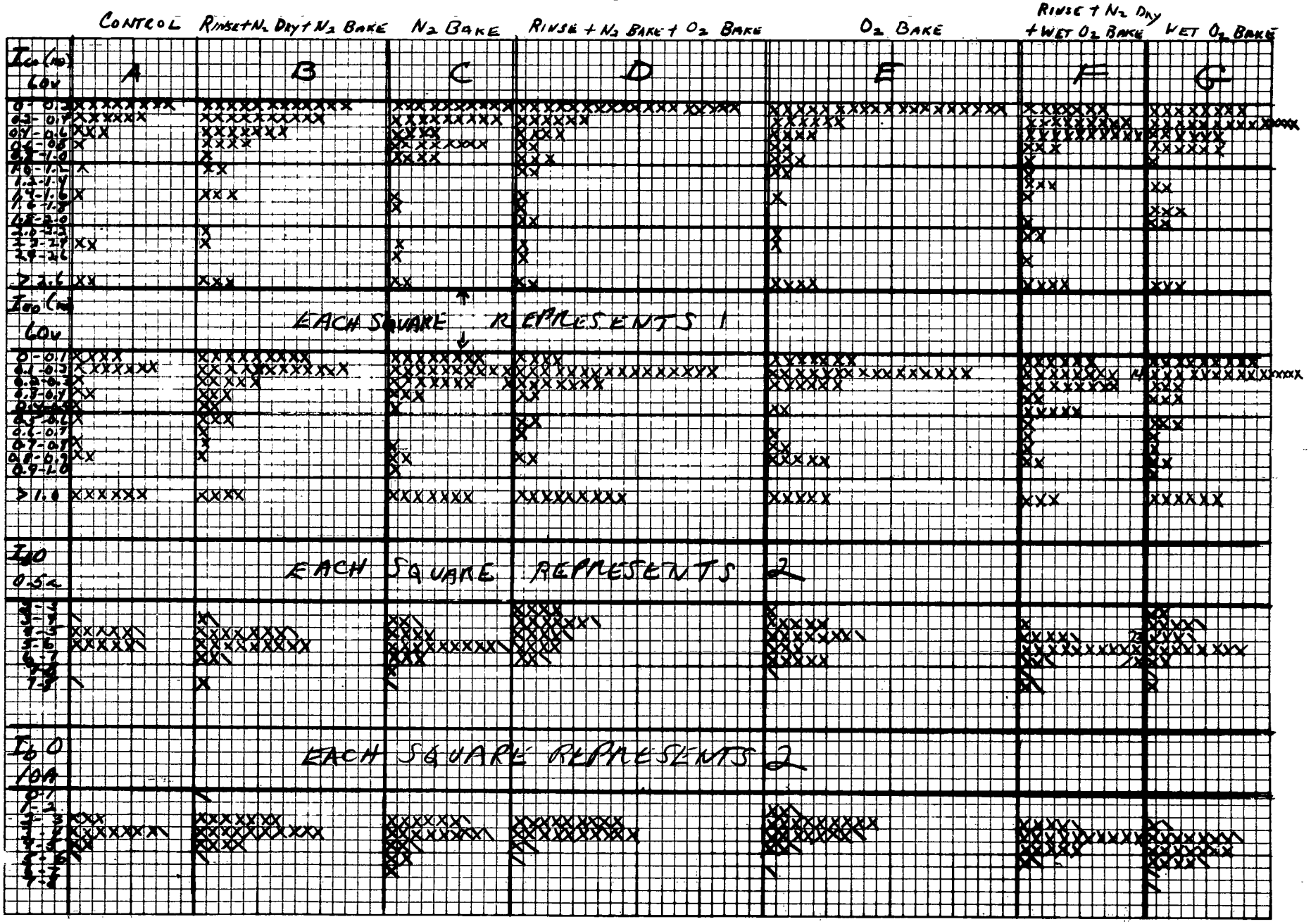
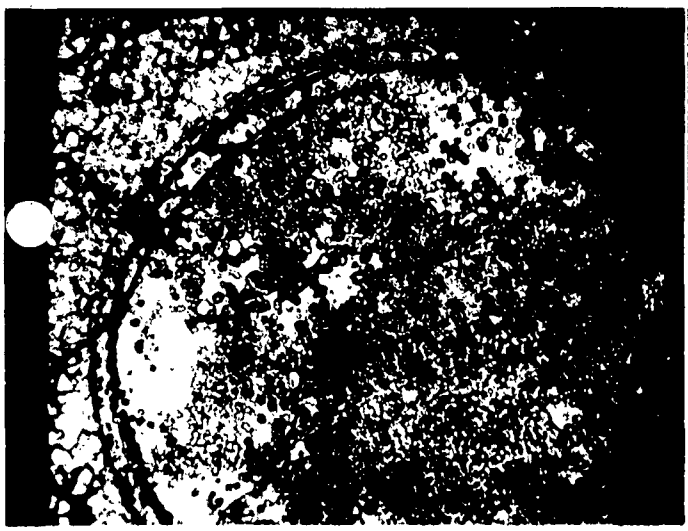
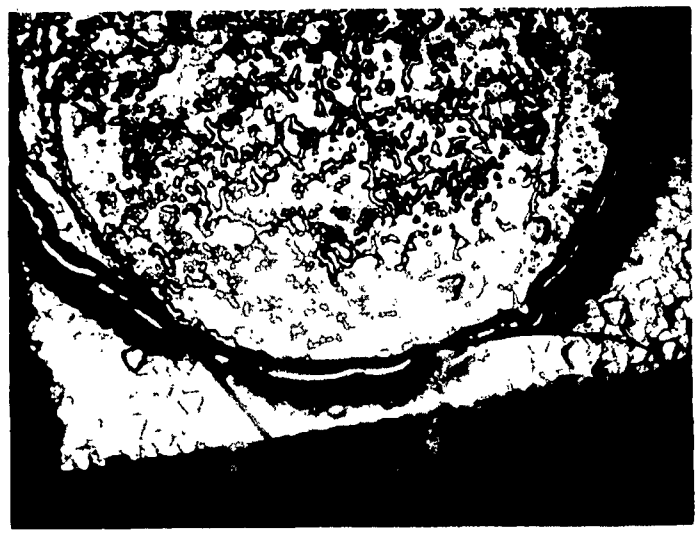
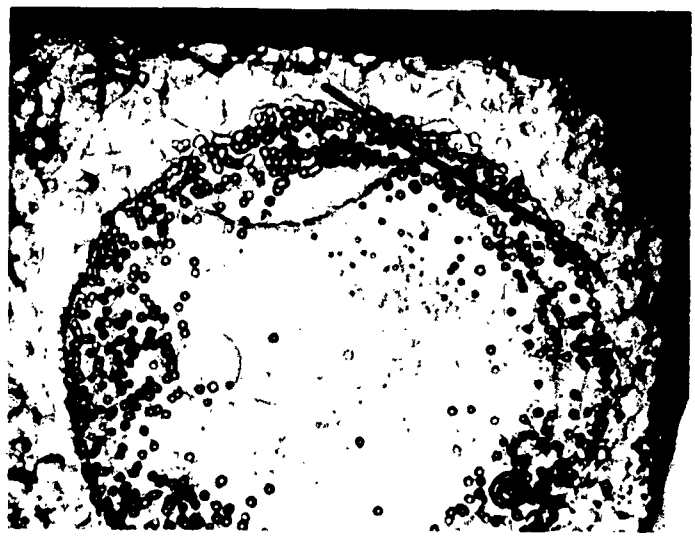


EXHIBIT 2

Exhibit 3







		Lot E 1-20 Coated		Lot G 1-20 Uncoated Control				
Silane		Pre-coat E 1-20	Pre-Coat Control G 1-20	After Coat E 1-20	Uncoated Control G 1-20	After Acetone E 1-20	After Cab E 1-20	After Cab G 1-20 Control
I_{EBO} @60v	<⊕.1			xxxxxxx	xxxxx	xxxxxxxxxx	xxxx	xxxxx
	>.1-.3			xxxx	xxxx	xxx	xxxxx	xxxx
	>.3-1			xx	xxx		xx	xxxxx
	>1-3	WET	WET	x	xxx		x	x
	>3				x	x	x	x
I_{EBO} @60v	<⊕.1			xxx	xxx	xxxxx	xxx	xxx
	>.1-.3			xxxxxx	xxxxxxx	xxx	xxxxxxx	xxxxxxxx
	>.3-1			xxx	xxxx	xxxx	x	x
	>1-3	WET	WET	xx	xx	xxxx	x	x
	>3				x	xx	x	x
I_B @ $C_{3v,2a}$	<10	xxxxxxxxxx	xxxxxxxx					
	10-20	xxxxx	xxxxxxx	xxxxxx	xxxxx	xxxxxxxx	xxxxxxxx	xx
	>20-30	x	x	xxxxxxx	xxxxxxxxx	xxxxxx	xxxxxx	xxxxxxxxx
	>30-50			x	xx	x	x	xxxx
	>50					x	x	

These Results Are Duplicated By Coating Lot E 21-40

Exhibit 4

LOT F-120 COATED LOT G-120 UNCOATED CONTROL

ETHYL SILICATE - THIN

		Coated F1-20	Control G1-20	Lab. atm. exp. wk'nd. F1-20	After Cap F1-20	After Cap G1-20 Control
	< 4.1	xxxx	xxxxx	xx	xxx	xxxxx
I_{CBO}	>.1-.3	xxxxxx	xxxx	xxxxxxxx	xxxxxx	xxxx
ma @ 60v	>.3-1	xxxxx	xxx	xxxx	xxxx	xxxxxx
	> 1-3	x	xxx	xx	xx	x
	> 3	x	x		x	
	< 4.1	x	xxx	xxxxx	xxx	xxx
I_{EBO}	> .1-.3	xxxxxx	xxxxxx	xxxxxxx	xxxxxxxxx	xxxxxxxx
ma @ 60v	>.3-1	xxxxxxx	xxxx	xx	xxxx	x
	> 1-3		xx	xx		xxx
	> 3	xx	x			x
	< 4 10					
I_B	>10-20	xxxxxxxxx	xxxxx	xxxxxxxx	xxxxx	xx
ma @	> 20-30	xxxxxxx	xxxxxxxxx	xxxx	xxxxxxxxxx	xxxxxxxxx
C 2v, 2a	> 30-50		xx	x		xxxx
	> 50					

EXHIBIT 5

CLEVITE TRANSISTOR

TEST DATA SHEET

DESCRIPTION OF TEST Storage Life PRODUCT TYPE R-6

TEST CONDITIONS 125°C or 100°C for 5000hrs DATE CODE

LOT SIZE LOT NUMBER 623

ALL TESTS ARE AT 25°C UNLESS OTHERWISE NOTED.

TEST	I_R @ V_{CE} = 2.0V, I_C = 3.0A						I_{CBO} @ V_{CB} = 40V or 65V						I_{EBO} @ V_{EB} = 12V						
UNITS	mA [42.8 – 87.5mA]						mA [<2.0mA]						mA [<0.5mA]						Helium Leak Test
CONDITION	initially																		4 Hr. Pressurization
HRS	0	100	500	1000	2500	5000	0	100	500	1000	2500	5000	0	100	500	1000	2500	5000	
1 X	72	73	74	77	81	83	.40	.66	.73	1.7	1.9	90†	.07	.05	.06	.07	.07	.07	2.6×10^{-8} std cc/sec
2 Z	66	68	70	72	73	73	.38	.76†	1.9†	6.0†	6.8†	4.0	.13	.12	.12	.13	.12	.12	1.9×10^{-8}
9 B	67	111	118	120	137	137	.60	.21	.21	.33	.32	.49	.09	.12	.23	.56	.60	.40	$>1.3 \times 10^{-5}$
16 A	54	76	82	82	82		.57	1.6	3.6	5.0	6.3		.08	.64	.68	.90	.90		8.0×10^{-7}
17 B	50	75	76	78	127		.16	.16	.16	.68	.46		.06	.08	.10	.13	.22		$>1.3 \times 10^{-5}$
20 B	56	57	59	58	60	61	.40	.60	.97	1.9	3.4	5.25	.08	.07	.07	.09	.08	.08	1.2×10^{-8}
26 Z	74	78	84	86	80	79	.18	.25	.24	.34	.34	.23	.38	.18	.66	3.2	2.7	.52	2.5×10^{-6}
37 B	46	46	44	44	170	153	.10	.10	.10	.16	7.0	1.6	.07	.06	.07	.07	22†	37†	1.4×10^{-8} → Rejects on Life
39 B	91	94	93	98	107	99	.60	.86	1.5	3.6	5.0	3.4	.08	.07	.07	.09	.08	.07	6.0×10^{-7}
50 B	57	60	71	76	168	172	.41	.42	.42	.54	15	.52	.07	.07	.09	.18	3.0	.24	$>1.3 \times 10^{-5}$
53 X	56	61	59	59	70	110	.73	.24	.80	1.2	5.4	10†	.09	.09	.09	.13	.34	22.5	8.2×10^{-7}
55 Z	86	97	128	135	142	163	.12	.13	.14	.26	.29	.18	.06	.06	.07	.09	.10	.10	1.3×10^{-6}
75 B	84	96	105	110	122	118	.11	.16	.22	.48	.75	.80	.06	.05	.10	.16	.25	.22	9.0×10^{-7}
78 A	72	80	120	125	136	150	.90	.94	.96	1.6	5.0†	3.8†	.38	.89†	.44†	.44†	23†	18	8.0×10^{-7}
98 B	70	72	76	75	80	81	.27	.28	.27	.39	.39	.31	.65	.88	.88	1.4	1.4	.88	3.2×10^{-7}
6																			
7																			
8																			
9																			
0																			
2 X	48	49	50	50	54		.10	.08	.07	.14	.14		.06	.06	.06	.07	.07		6.0×10^{-9} std cc/sec
3 Z	48	45	44	44	46	47	.11	.13	.16	.22	.24	.32	.04	.03	.03	.04	.04	.06	5.0×10^{-9}
5 B	46	46	50	50	52	52	.18	.18	.20	.31	.32	.28	.04	.04	.04	.05	.05	.04	4.0×10^{-9}
7 A	50	47	47	47	49	53	.10	.10	.10	.16	.16	.14	.06	.06	.06	.07	.07	.07	2.6×10^{-7}
8 B	93	97	100	99	99	99	.18	.20	.22	.32	.25	.25	.18	.13	.13	.17	.17	.14	$>1.3 \times 10^{-5}$
10 6	75	73	70	72	78	81	.18	.20	.22	.36	.36	.25	.05	.05	.05	.06	.06	.06	4.0×10^{-9}
11 7	67	68	73	76	81	82	.08	.08	.09	.20	.36	.15	.05	.07	.08	.10	.11	.07	5.0×10^{-9} → Good on Life
14 B	58	60	68	72	82	81	.10	.09	.10	.14	.14	.14	.08	.02	.17	.26	.26	.22	6.7×10^{-8}
15 B	81	78	76	76	75	78	.15	.22	.24	.38	.42	.42	.08	.07	.07	.07	.07	.06	4.0×10^{-9}
19 B	54	53	59	63	64	66	.33	.32	.32	.44	.46	.46	.18	.17	.18	.24	.24	.18	3.3×10^{-8}
20 Y	46	69	74	76	77	74	.51	.22	.26	.36	.43	.30	.13	.09	.14	.20	.23	.20	$>1.3 \times 10^{-5}$
23 Z	72	70	72	75	78	80	.16	.12	.12	.14	.14	.14	.11	.10	.12	.14	.14	.13	6.0×10^{-9}
25 B	56	54	54	56	58	57	.10	.10	.11	.19	.22	.15	.06	.05	.05	.06	.05	.05	1.3×10^{-9}
28 A	54	52	62	66	68	69	.11	.10	.16	.28	.38	.27	.05	.06	.06	.16	.29	.20	4.4×10^{-8}
5																			
6																			
7																			
8																			
9																			
0																			

MEAN AND STANDARD DEVIATION OF
ICBO & HFE VS. 1000 HR. LIFE
2N456A

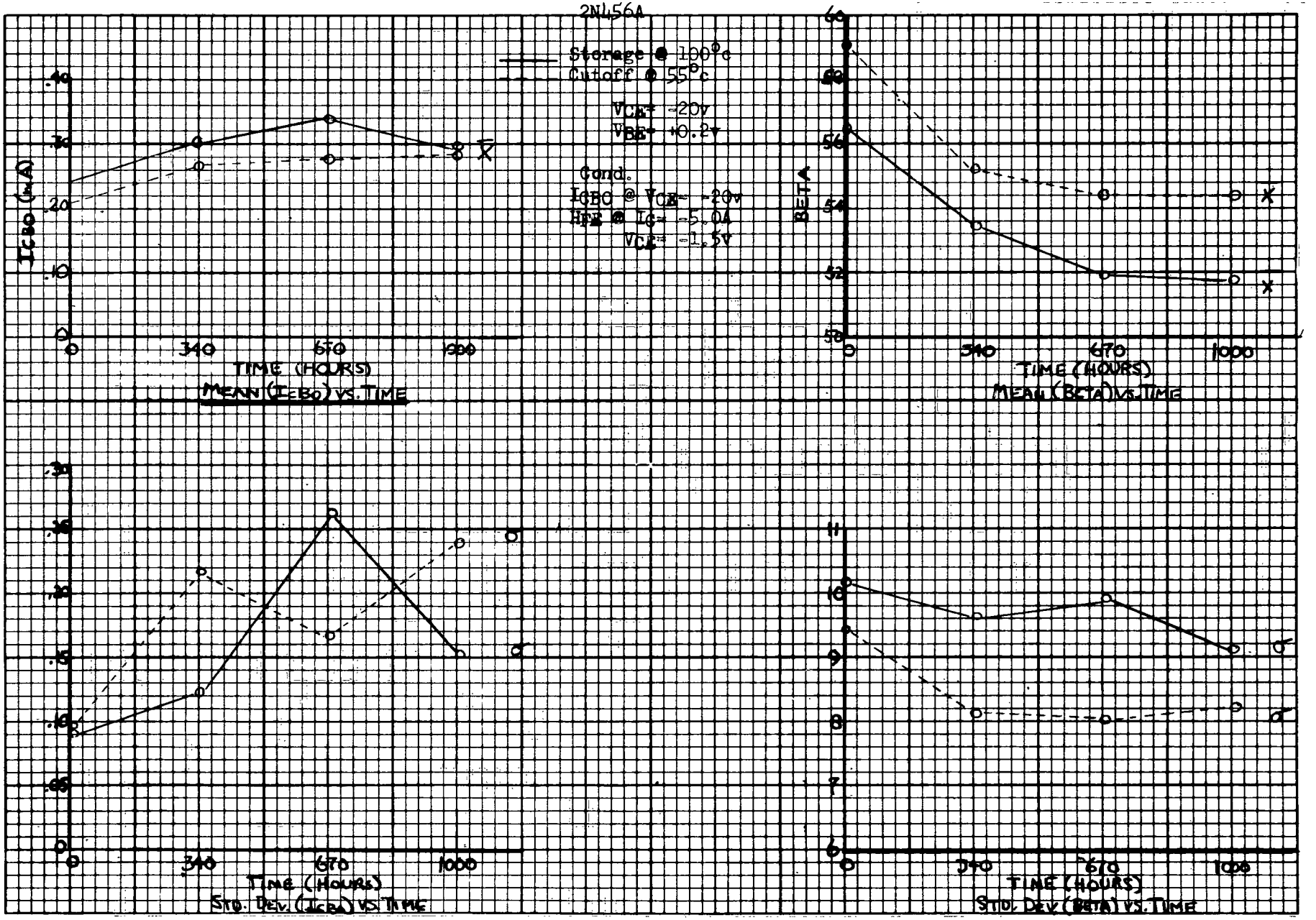


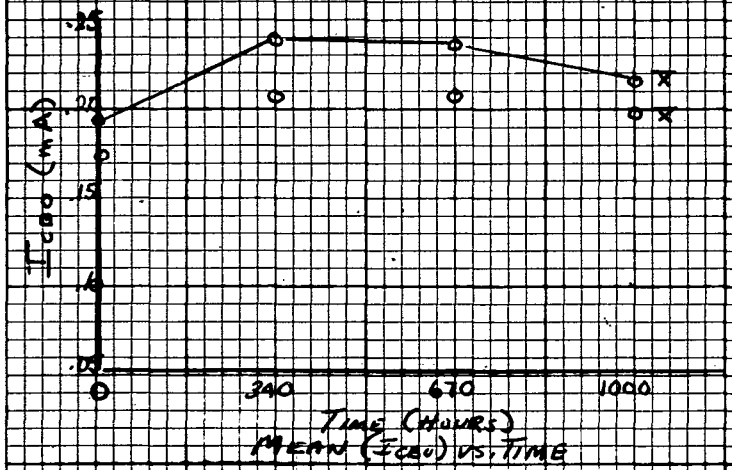
Exhibit 7

MEAN AND STANDARD DEVIATION OF I_{CBO} & H_{FE} VS. 1000 HR. LIFE

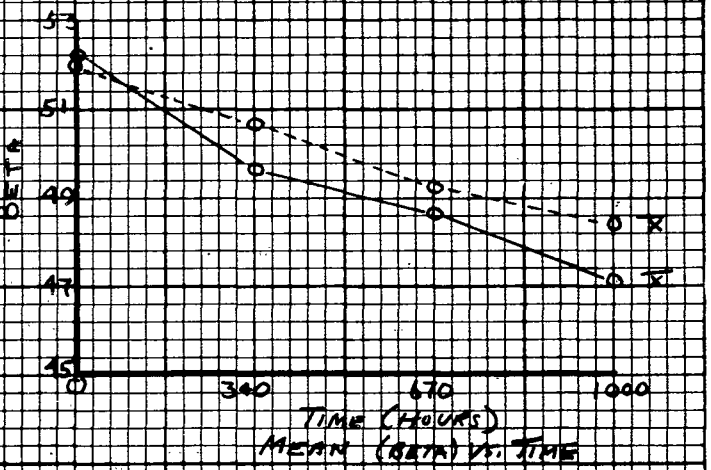
2N457A

STORAGE @ 100°C.
CUTOFF @ 55°C.
$V_{CE} = -30V$
$V_{BE} = +0.2V$

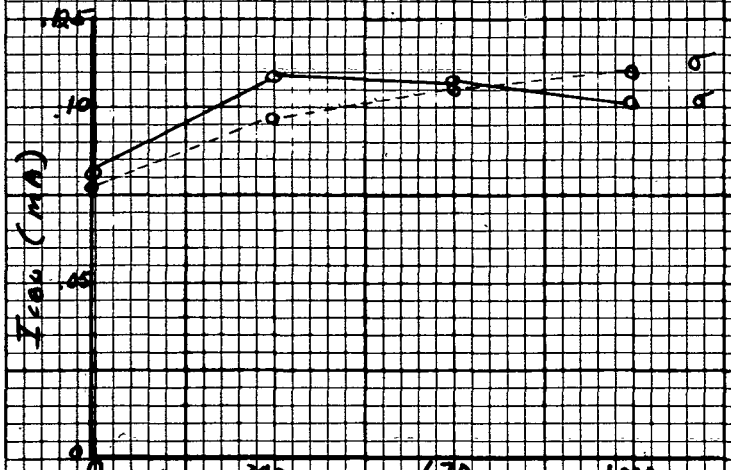
COND.
I_{CBO} @ $V_{CE} = -30V$
H_{FE} @ $I_C = -5.0A$
$V_{CE} = -1.5V$



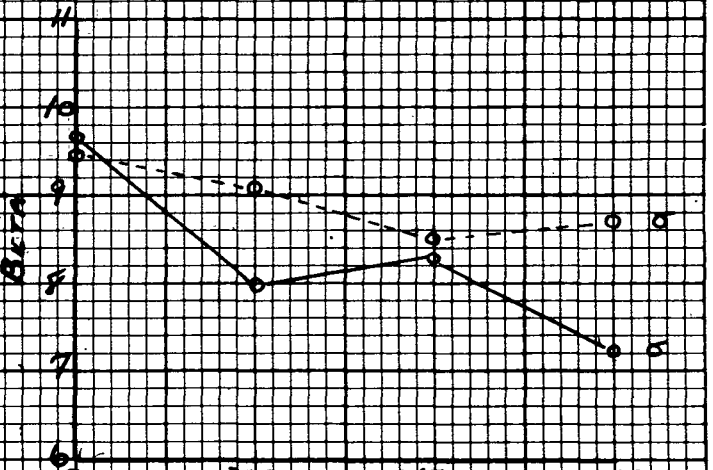
MEAN (I_{CBO}) VS. TIME



MEAN (BETA) VS. TIME



STD. DEV. (I_{CBO}) VS. TIME



STD. DEV. (BETA) VS. TIME

EXHIBIT B

MEAN + STANDARD DEVIATION OF
I_{CBO} & H_{FE} VS. 1000 HOUR LIFE
2N458A

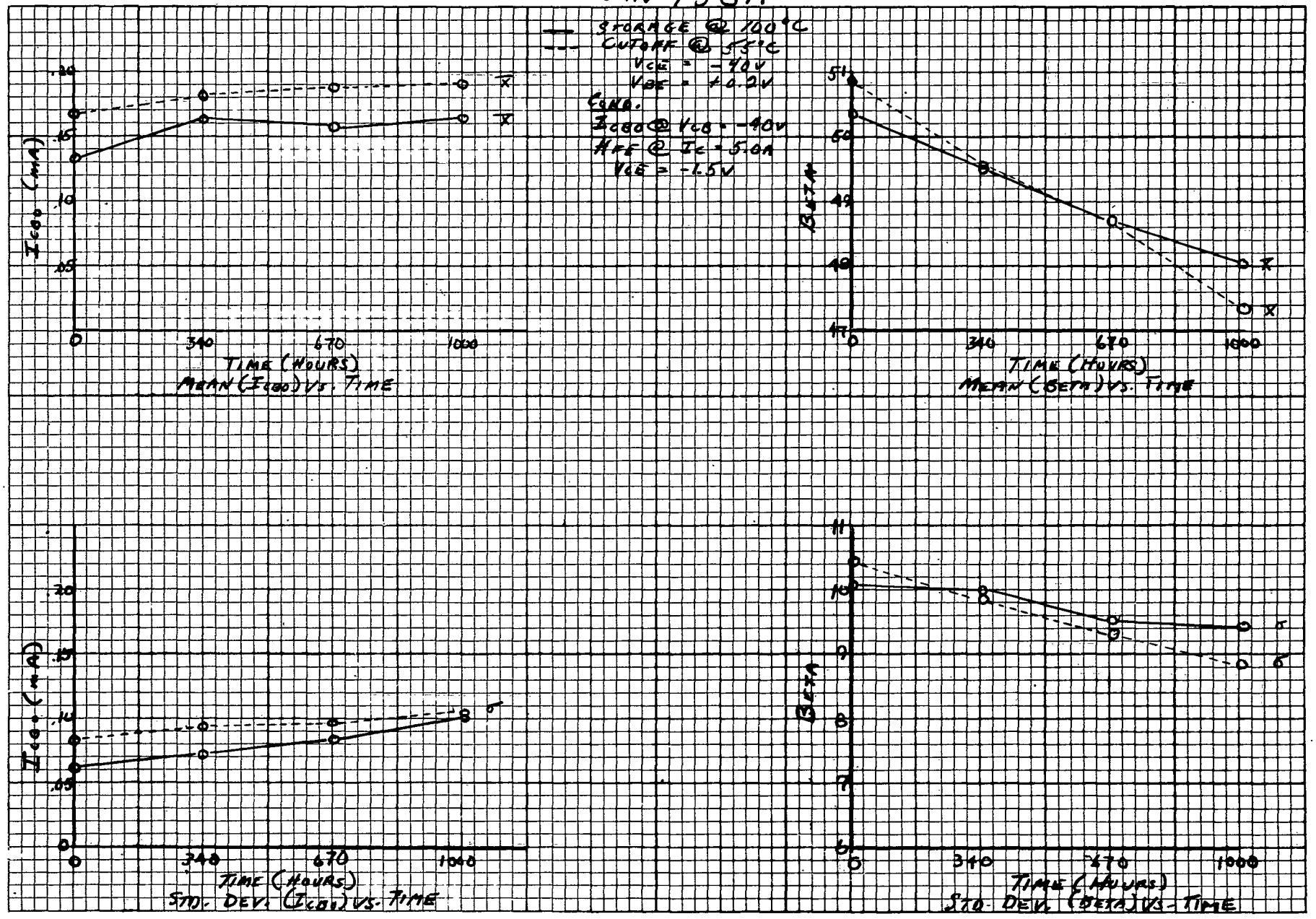


EXHIBIT 9